Remarks

The applicant respectfully requests reconsideration of the present U.S. Patent application as amended herein. Claims 2, 5, 17, 20, 21, and 32 have been amended. Claim 6 has been canceled, while claims 42 and 43 have been added. Thus, claims 2-5 and 7-43 are pending.

Objections to the Specification

The abstract was objected to as being shorter than fifty words. The abstract has been amended and its length now falls within the required 50-150 words. A replacement sheet with the amended abstract paragraph is attached and the applicant requests that the examiner withdraw his objection.

Objections to the Claims

Claim 6 was objected to for a typographical error but has since been cancelled. Hence, the objection is moot.

Claim Rejections – 35 U.S.C. § 102

Claims 2 and 17

Claims 2 and 17 were rejected under 35 U.S.C. § 102(e) as being anticipated by Grisamore, U.S. Patent 6,535,901. However, the applicant submits that Grisamore does not anticipate claims 2 and 17 because it does not disclose a pipelined reduction pattern. Nor does Grisamore disclose a reduction pattern structured by maximally partitioning

input bits of equal significance into groups of three to serve as inputs to full-adders, remaining groups of two to serve as inputs to half-adders, and remaining single bits to serve as inputs to single registers.

The language of claim 2 is as follows:

> ...
> a multi-stage series of Boolean function generators coupled with the inputs to implement one or more full-adders, half-adders, and single registers to produce intermediate summation results by combining the input terms according to a pipelined reduction pattern to be structured such that input bits of equal significance are maximally partitioned into groups of three to serve as inputs to full-adders, remaining groups of two to serve as inputs to half-adders, and remaining single bits to serve as inputs to single registers...

Claim 17 similarly recites a pipelined series of full-adders, half-adders, and single registers structured in such a way as to pass groups of three bits of equal significance as inputs to full-adders with remaining groups of two passed as inputs to half-adders and remaining single bits passed directly to registers.

Grisamore, on the other hand, does not disclose pipelined adder tree reduction stages. This is made clear by the fact that Grisamore does not include any registers between adders like those depicted by item 308 in Fig. 3 of the present patent application. In fact, Grisamore teaches that the entire reduction tree is to serve as a single pipeline stage (col. 3, lines 2-7). Referring to Grisamore's Fig. 1, the current partial products are fed into the reduction tree to produce the first and second current resultants. They are then fed back into the reduction tree as the first and second preceding resultants in the "next cycle." By Grisamore's description it is clear that an entire cycle is devoted to allowing partial products to trickle down through the multiple reduction stages of the

reduction tree, which are shown in Grisamore's Fig. 5. In contrast to Grisamore, claims 2 and 17 disclose a pipelined reduction tree.

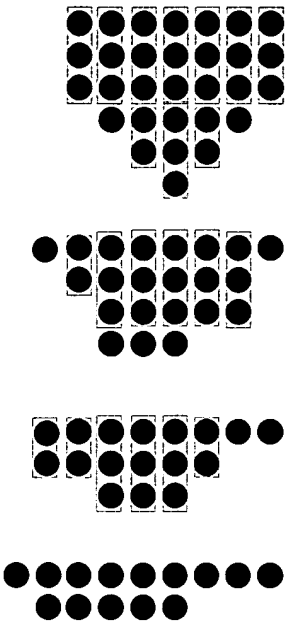
The Office Action cites col. 1, lines 36-38 as teaching the registers recited in claims 2 and 17. However, those lines do not refer to the reduction tree as disclosed by Grisamore, but rather to a pipelined array multiplier, which has a completely different architecture.

Just as Grisamore fails to disclose pipelined adder tree reduction stages, it also fails to disclose the reduction tree structured to *maximally* partition bits of equal significance into groups of three to serve as inputs to full-adders with remaining groups of two serving as inputs to half-adders and remaining single bits as inputs to registers. This deficiency is seen most clearly in Grisamore's Fig. 5 and the corresponding discussion in col. 4, line 64 through col. 6, line 28. There, Grisamore describes reducing the height of input columns (bits of equal significance) from 6 to 4 to 3 to 2. Fig. 5 shows in the first reduction stage that groups of three bits are formed in columns 4 and 5 to serve as inputs to full-adders, but this partitioning is not done *maximally*. That is, groups of three bits could have been formed in columns 2, 3, and 6 as well as an additional group of three in column 4, but Grisamore explicitly discloses not to do so.

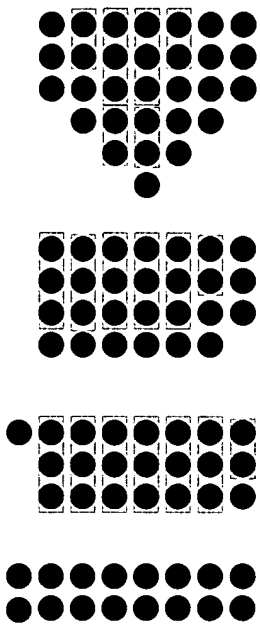
Fig. 5 goes on to show that some groups of two are formed to serve as inputs to half-adders, but again, this is not done to the fullest possible extent. A side-by-side comparison of the resulting structure of the reduction tree using the claimed manner of maximally partitioning bits into groups of three, then two, and then one at each reduction stage versus Grisamore's reduction tree is illustrative. Of course groups of three and two are summed by full-adders and half-adders, respectively, leading to one sum bit in the

same column of the next reduction stage and one carry bit in the column to the left in the next stage. Single bits are passed straight down into registers.

Present Invention



Grisamore (Fig. 5)



Clearly, the reduction stages of the present invention are different than Grisamore's reduction stages, culminating in resultants of a different form. Namely, the first three columns of the end resultants need not be summed at all using the applicant's apparatus.

In summary, the applicant submits that Grisamore does not disclose a pipelined reduction tree or structuring the reduction tree by maximally partitioning bits of equal significance into groups of three, then two, then one, to serve as inputs to full-adders, half-adders, and registers, as recited in claims 2 and 17. Therefore, the applicant submits that Grisamore does not anticipate claims 2 and 17.

Claims 3, 5, 7-9, 18, and 20-24

Claims 3, 5, 7-9, 18, and 20-24 were also rejected as being anticipated by Grisamore. However, each of these claims depends from and includes the limitations of either claim 2 or 17 and is not anticipated by Grisamore for at least the reasons set forth with respect to the corresponding independent claims.

Claim Rejections – 35 U.S.C. § 103

Claim 32

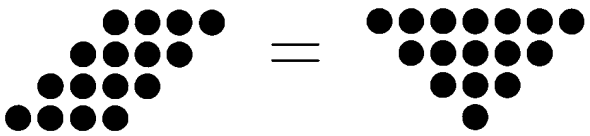
Claim 32 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Grisamore in view of the admitted prior art. However, the applicant submits that no combination of Grisamore with the admitted prior art teaches simultaneously passing the partial products from both terms resulting in real components, or both terms resulting in imaginary components, during a complex multiply into an adder tree composed of full-adders, half-adders, and registers structured based on some attribute of the input terms.

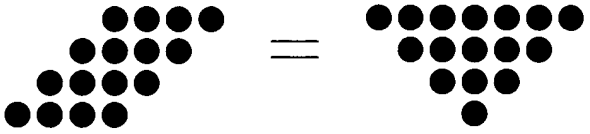
Claim 32 recites a method for performing complex multiplication with the following steps:

generating a plurality of partial products from two or more input terms;
for a real-component branch, negating certain partial products and simultaneously passing the negated and non-negated partial products to a multi-stage series of Boolean function generators that implements one or more full-adders, half-adders, and single registers to produce intermediate summation results by combining the partial products, the structure of the Boolean function generators to be determined based, at least in part, on one or more attributes of the input terms;
for an imaginary-component branch, simultaneously passing the partial products from the two or more input terms to a multi-stage series of Boolean function generators that implements one or more full-adders, half-adders, and single registers to produce

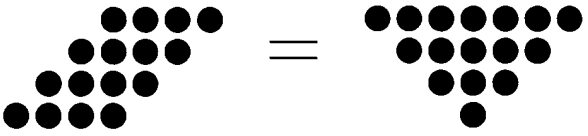
intermediate summation results by combining the partial products, the structure of the Boolean function generators to be determined based, at least in part, on one or more attributes of the input terms...

It is well known that a complex multiply of the form (a + jb) * (c + jd) equals (ac – bd) + j(ad + bc). Furthermore, Grisamore discloses a method of passing the partial products resulting from the multiplication of two inputs into a reduction tree consisting of full-adders and half-adders in some arrangement. Grisamore also discloses passing accumulator bits from a previous multiply into the reduction tree. It follows that in order to accomplish a complex multiply of the form shown above Grisamore's multiply accumulator would have to follow these steps (the partial products for each step are shown for the case of 4-bit numbers):

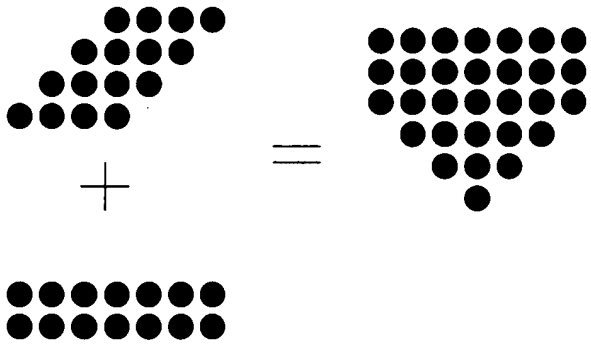
1) Calculate ac 

2) Calculate bd; 

3) Subtract bd from ac (the feedback paths for accumulator bits shown in Grisamore's Fig. 1 could not be used in this case because bd would have to be negated first).

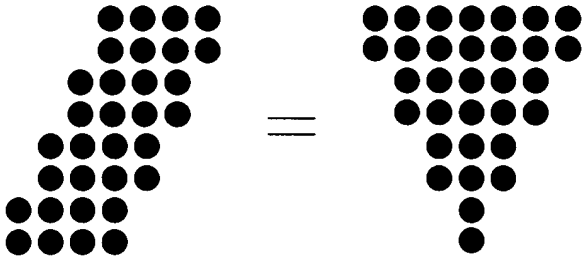
4) Calculate ad 

5) Calculate bc and add to the resultants from ad simultaneously (here the accumulator feedback can be used since bc and ad are simply added)

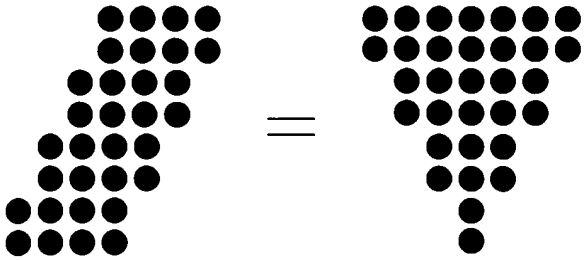


However, claim 32 recites feeding the partial products for both terms resulting in real components into the reduction tree simultaneously. Likewise, both terms resulting in an imaginary component are fed into the reduction tree simultaneously. Hence, applicant's arrangement of partial products would appear as follows:

1) Feed the partial products for ac and the negated bd partial products into the reduction tree simultaneously



2) Feed the partial products for ad and bc into the reduction tree simultaneously



It is clear from the illustrations that the two methods for performing a complex multiply are different. Namely, Grisamore does not input the partial products from two terms to be accumulated into the reduction tree simultaneously. Furthermore, the admitted prior art does not disclose simultaneous input of the partial products from two terms to be accumulated into the reduction tree, as recited in the claim. Since no combination of Grisamore with the admitted prior art teaches or suggests these limitations of claim 32, the applicant submits that claim 32 is patentable over the references.

Claims 4, 10-16, 19, 25-31, and 33-41

Claims 4, 10-16, 19, 25-31, and 33-41 were rejected as being unpatentable over various combinations of Grisamore, Chang et al., Fang et al., and the admitted prior art. However, each of claims 4, 10-16, 19, 25-31, and 33-41 depends from and includes the limitations of one of independent claims 2, 17, and 32. Moreover, Chang, Fang, and the admitted prior art are not cited to teach or suggest, nor do they teach or suggest, the argued deficiencies of Grisamore with respect to independent claims 2, 17, and 32. Therefore, claims 4, 10-16, 19, 25-31, and 33-41 are patentable over the references for at least the same reasons as set forth with respect to their corresponding independent claims.

New Claims

Claims 42 and 43

Claims 42 and 43 recite limitations similar to those that have already been discussed with regard to pipelined reduction stages and maximally partitioning input bits of equal significance into full-adder inputs, then half-adder inputs, and then single register inputs. Therefore, the applicant submits that claims 42 and 43 are patentable over the references for at least the same reasons as set forth previously in this response.

CONCLUSION

For at least the foregoing reasons, the applicant submits that the rejections have been overcome. Therefore, claims 2-5 and 7-43 are in condition for allowance and such action is earnestly solicited. The examiner is respectfully requested to contact the undersigned by telephone if such contact would further the examination of the present application. Please charge any shortages and credit any overcharges to our Deposit Account number 02-2666.

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, LLP

Date: 8/19/04

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Annotated Sheet Showing Changes

FIG. 4

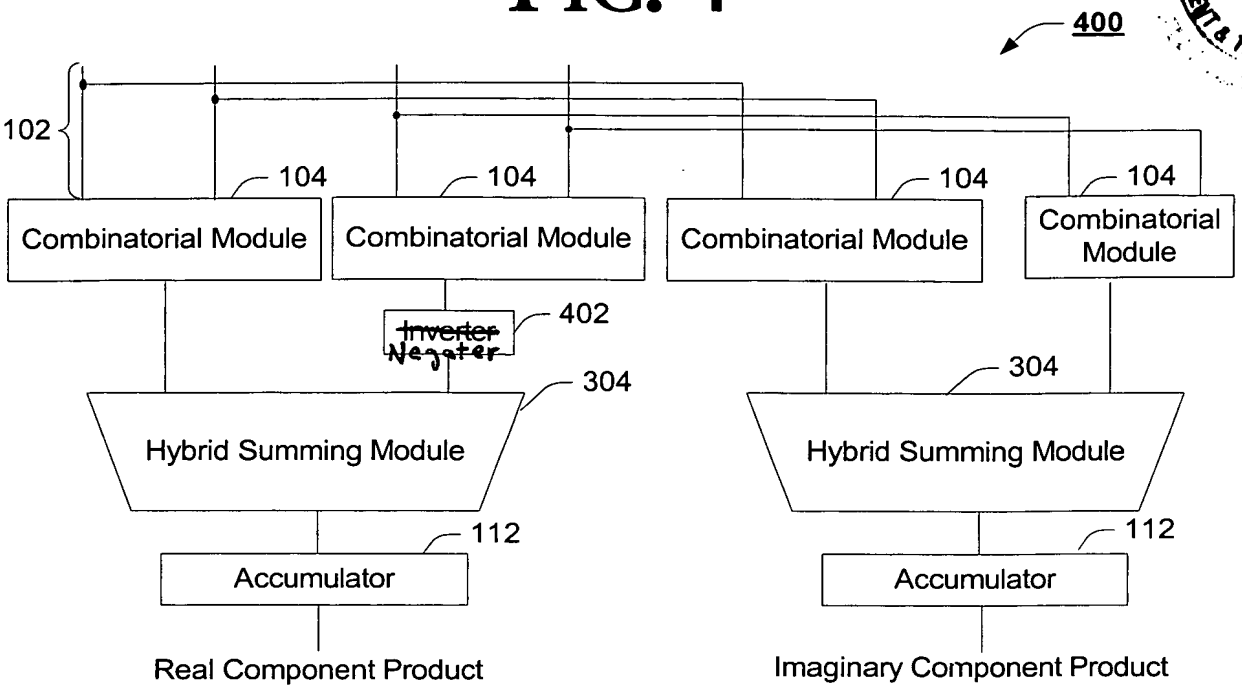

FIG. 5